Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] An apparatus for eliminating time delay errors during automatic testing of electronics, using automatic test equipment comprising:

device interface board wiring having a device interface board signal time delay;

a device socket connected to said device interface board wiring, having a device socket signal time delay;

first channel and second channel pin electronics wiring connected to said device interface board wiring, having pin electronics signal time delays;

a first channel including a set of driver electronics, said set of driver electronics including inputs for receiving drive data, drive timing edge source data, and a first channel output, said first channel output transmitting information to a device under test through said first channel pin electronics, said device interface board wiring, and said device socket;

a second channel having a set of receiver electronics, said set of receiver electronics including inputs for comparison data source information, comparison timing edge source information, and an output from said device under test; and

a compiler to automatically route said drive timing edge source data, signal levels, and data to said first channel, and said comparison timing edge source information, signal levels, and data to said second channel;
said first and second channels separate and distinct from one another and compensating for time delay errors when said device under test is electronically exercised.

[c2] The apparatus of claim 1 wherein said time delay errors comprise round-trip timing errors from said automatic test equipment to said device under test, and from said device under test to said automatic test equipment.

[c3] The apparatus of claim 2 wherein said time delay errors comprise a summation of said pin electronics signal time delays, said device interface board signal time delay, and said device socket time delay.

[c4] The apparatus of claim 1 wherein said first channel and second channel pin electronics signal time delays are approximately equal.

[c5] The apparatus of claim 1 wherein said set of receiver electronics includes a comparator.

[c6] The apparatus of claim 1 wherein at least one of said second channel inputs is electrically connected to said first channel output through said first and second chan-

nel pin electronics wiring and said device interface board wiring.

[c7] The apparatus of claim 1 further including a set of receiver electronics in said first channel and a set of driver electronics in said second channel.

[c8] A method for eliminating time delay errors during automatic testing of a device under test comprising:
separating drive and compare waveforms onto first and second channels of electronics;
routing drive timing edge source data, signal levels, and data to said first channel;
routing comparison timing edge source information, signal levels, and data to said second channel; and
compensating for said time delay errors when testing said device under test.

[c9] The method of claim 8 wherein said routing further includes programming an automatic test equipment compiler to configure internal signal switches to force all drive edges and waveforms to occur on said first channel and all compare waveforms to occur on said second channel.

[c10] The method of claim 9 further comprising applying said drive edge waveforms and said compare waveforms in a

vector file identifying an appropriate tester cycle type and drive or compare data.

[c11] The method of claim 8 further including self-calibrating automatic test equipment for all pins, and nulling out any delays due to wiring.

[c12] The method of claim 9 further including eliminating overlap of edges and data induced by implementing auto-correction schemes of said automatic test equipment's self-calibration using TDR delays.

[c13] A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for negating time delay errors during automatic testing of a device under test, said method steps comprising:
separating drive and compare waveforms onto first and second channels of electronics;
routing drive timing edge source data, signal levels, and data to said first channel;
routing comparison timing edge source information, signal levels, and data to said second channel; and
compensating for said time delay errors when testing said device under test.